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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,658	12/12/2001	Scott Derner	400.105US01	7933

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FOGG, SLIFER & POLGLAZE, P.A.  
P.O. Box 581009  
Minneapolis, MN 55458-1009

EXAMINER

NGUYEN, TAN

ART UNIT	PAPER NUMBER
	2818

DATE MAILED: 09/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/017,658

Applicant(s)

DERNER ET AL.

Examiner

Tan T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM

THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1)  Responsive to communication(s) filed on \_\_\_\_.
- 2a)  This action is FINAL. 2b)  This action is non-final.
- 3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4)  Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5)  Claim(s) 9-13 is/are allowed.
- 6)  Claim(s) 1-8 and 14-22 is/are rejected.
- 7)  Claim(s) \_\_\_\_ is/are objected to.
- 8)  Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9)  The specification is objected to by the Examiner.
- 10)  The drawing(s) filed on 12/12/01 is/are: a)  accepted or b)  objected to by the Examiner. Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11)  The proposed drawing correction filed on \_\_\_\_ is: a)  approved b)  disapproved by the Examiner. If approved, corrected drawings are required in reply to this Office action.
- 12)  The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All b)  Some \* c)  None of:
    1.  Certified copies of the priority documents have been received.
    2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_.
    3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14)  Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
  - a)  The translation of the foreign language provisional application has been received.
- 15)  Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1)  Notice of References Cited (PTO-892)
- 2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3)  Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_.

- 4)  Interview Summary (PTO-413) Paper No(s) \_\_\_\_.
- 5)  Notice of Informal Patent Application (PTO-152)
- 6)  Other: \_\_\_\_\_

1. The Information Disclosure Statement submitted by Applicants on February 12, 2002 has been received and fully considered.
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-4, 8, 14-17, 21-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Takasugi (U.S. Patent No. 5,418,739).

Takasugi disclosed in figure 1 a memory device having a plurality of unit column circuits [30<sub>1</sub>-30<sub>i+2</sub>], wherein each unit column circuit having a plurality of bit lines pairs [BL<sub>i</sub>, BL<sub>i</sub>/], one bit line [BL<sub>i</sub>] is connected to the memory cells [31<sub>1i</sub>, 31<sub>3i</sub>, 31<sub>5i</sub> ..] at odd number positions, the other bit line [BL<sub>i</sub>/] is connected to the memory cells [31<sub>2i</sub>, 31<sub>4i</sub>, 31<sub>6i</sub> ..] at even number positions (column 5, lines 62-68). The bit line pair [BL<sub>i</sub>, BL<sub>i</sub>/] is coupled to a sense amplifier [32<sub>i</sub>] to form a differential sensing circuit. Takasugi also disclosed first and second voltage lines, namely, a power supply line [33<sub>i</sub>] (VCC) and a ground line [33<sub>i</sub>/] (VSS) are provided in each of the unit column circuits [30<sub>i</sub>]. The power supply lines [33<sub>i</sub>] and the ground line [33<sub>i</sub>/] are selectively connected with nodes between the capacitor [31a] and the transfer gate [31b] in the memory cell [31<sub>ki</sub>] serving as a ROM cell. The memory cells in which those lines [33<sub>i</sub>, 33<sub>i</sub>/] are not connected to the nodes thereof serve as ordinary DRAM memory cells. The power supply line [33<sub>i</sub>] and the ground line [33<sub>i</sub>/] feed respective voltages to the selected memory cells as

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stored data, corresponding to either "1" or "0", to make the memory cells acts as ROM cell (column 6, lines 21-33).

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 5-7, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takasugi in view of Holland (U.S. Patent No. 5,995,409) or Jung et al. (U.S. Patent No. 6,327,174).

See description of Takasugi in paragraph 3, supra. Holland disclosed in the Abstract that by grounding a first capacitor plate of a DRAM cell, and applying a programming voltage to a second capacitor plate, the dielectric disposed between the first capacitor plate and the second capacitor plate breaks down, thereby shorting the first and second capacitor plates.

Jung disclosed et al. disclosed in the Abstract that a DRAM cell having an ONO stack layer is used as a dielectric film of a capacitor of the DRAM cell. When a supply power is over 6 volts, the dielectric layer would be breakdown so that leakage is occur between a lower electrode and an upper electrode of the capacitor. The DRAM cell which can be used as a ROM cell.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the programming method of Holland or Jung et al. to the DRAM cells of Takasugi.

The rationale is as follows: A person of ordinary skill in the art would have been motivated to apply the programming method of Holland or Jung et al. since the same fabrication process is being used, both the EPROM and DRAM cells can be provided on a single chip (Holland, column 3, lines 38-40).

6. Claims 9-13 are allowed.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Koga is cited to show one time programmable read only memory programmed by destruction of insulating layer.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (703) 308-1298. The examiner can normally be reached on Monday to Friday from 08:00 AM to 04:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms, can be reached on (703) 308-4910. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.



Tan T. Nguyen  
Primary Examiner  
Art Unit 2818  
September 11, 2002